

5      **WHAT IS CLAIMED IS:**

1.      A semiconductor sensor comprising:  
a first single crystal silicon wafer layer;  
a single crystal silicon structure formed in said first wafer layer and  
including two oppositely disposed substantially vertical major surfaces and  
10 including two oppositely disposed generally horizontal minor surfaces wherein  
the aspect ratio of major surface to minor surface is at least 5:0; and  
a carrier including a recessed region, wherein said carrier is secured to  
said first wafer layer such that said structure is suspended opposite the recessed  
region.  
15
2.      The sensor of claim 1,  
wherein said carrier includes a silicon wafer layer; and  
wherein said first layer and said carrier are fusion bonded together.
- 20 3.      The sensor of claim 1 wherein said first layer is formed of  
<100> oriented silicon crystal.
4.      The sensor of claim 1 wherein the aspect ratio of major surface  
to minor surface is at least 20:1.
- 25 5.      The sensor of claim 1 wherein said structure is a beam secured  
at only one end thereof to said first wafer layer.
6.      The sensor of claim 1 wherein said structure is a beam secured  
30 at one end thereof to said first wafer layer and including a seismic mass at the  
other end thereof.

FOOTNOTES

5           7.     The sensor of claim 1 wherein said structure is a beam secured  
at one end thereof to said first wafer layer and including an electronic circuit  
formed in the other end thereof.

10           8.     The sensor of claim 1,  
wherein said first layer is formed of <100> oriented silicon crystal; and  
wherein said structure is a beam secured at one end thereof to said first  
wafer layer and including an electronic circuit formed in the other end thereof.

15           9.     The sensor of claim 1 wherein said structure is a beam secured  
at one end thereof to said first wafer layer and including a plurality of vertical  
plates formed in the other end thereof.

20           10.    The sensor of claim 1,  
wherein said structure is a beam secured at one end thereof to said first  
wafer layer and including a plurality of vertical plates formed in the other end  
thereof; and  
wherein said vertical plates have an aspect ratio of at least 10:1.

25           11.    The sensor of claim 1,  
wherein said structure is a beam secured at one end thereof to said first  
wafer layer and including a plurality of vertical plates formed in the other end  
thereof and further including an electronic circuit formed in the other end  
thereof.

30           12.    The sensor of claim 1,  
wherein said first layer is formed of <100> oriented silicon crystal; and

09923194-104101  
TOTAL 4672260

5            wherein said structure is a beam secured at one end thereof to said first wafer layer and including a plurality of vertical plates formed in the other end thereof and further including an electronic circuit formed in the other end thereof.

10           13.    The sensor of claim 1,  
             wherein said first layer is formed of <100> oriented silicon crystal;  
             wherein said structure is a beam secured at one end thereof to said first wafer layer and including a plurality of vertical plates formed in the other end thereof and further including an electronic circuit formed in the other end  
15           thereof; and  
             wherein said vertical plates have an aspect ratio of at least 10:1.

             14.    The sensor of claim 1 wherein said structure is a beam secured at both ends thereof to said first wafer layer.

20           15.    The sensor of claim 1 wherein said structure is a plate secured at only one end thereof to said first wafer layer.

             16.    A semiconductor sensor comprising:  
25           a first single crystal silicon wafer layer;  
             a curvilinear single crystal silicon structure formed in said first wafer layer and including two generally opposite facing first substantially vertical surface portions and two generally opposite facing first generally horizontal surface portions; and

5           a second single crystal wafer layer including a recessed region wherein  
said second wafer layer is secured to said first wafer layer such that said  
structure is suspended opposite the recessed region.

10           17.    The sensor of claim 16 wherein said first wafer layer and said  
second wafer layer are fusion bonded together.

18.    The sensor of claim 16 wherein said first layer is formed of  
<100> oriented silicon crystal.

15           19.    The sensor of claim 16 wherein the aspect ratio of the first  
substantially vertical surface portions to the first generally horizontal surface  
portions is at least 5:1.

20           20.    The sensor of claim 16 wherein the aspect ratio of the first  
substantially vertical surface portions to the first generally horizontal surface  
portions is at least 20:1.

25           21.    The sensor of claim 16,  
              wherein said structure further includes two generally opposite facing  
second substantially vertical surface portions and two generally opposite facing  
second generally horizontal surface portions; and  
              wherein the aspect ratio of the first substantially vertical surface  
portions to the first generally horizontal surface portions differs from the aspect  
ratio of the second substantially vertical surface portions to the second  
30           generally horizontal surface portions by at least 2:1.

09928194-034101  
FOI b3 b6 b7C b7E

5           22.     The sensor of claim 16 wherein said first substantially vertical portion has a height of at least 10 microns.

          23.     A semiconductor sensor comprising:  
          a first single crystal silicon wafer layer;  
10         a single crystal silicon structure formed in said first wafer layer and including two substantially vertical surfaces and two generally horizontal surfaces wherein a height of the vertical surfaces is substantially uniform and wherein a width of the horizontal surfaces is nonuniform; and  
          a carrier including a recessed region wherein said carrier is secured to  
15         said first wafer layer such that said structure is suspended opposite the recessed region.

          24.     A semiconductor sensor comprising:  
          a first single crystal silicon wafer layer;  
20         a plurality of single crystal silicon plates formed in said first wafer layer and having an aspect ratio of at least 10:1; and  
          a second single crystal wafer layer secured to said first wafer layer such that said plates are suspended over the second wafer layer.

25         25.     The sensor of claim 1 wherein,  
          said second wafer layer defines a recessed region and said plates are suspended opposite the recessed region.

          26.     The sensor of claim 24 wherein said first layer and said second  
30         layer are fusion bonded together.

FOIA b 7 - D

5

10

15

20

25

30

34. The sensor of claim 29,

5            wherein at least one of said plurality of beams includes a plurality of  
vertical plates formed therein; and  
             wherein said vertical plates have an aspect ratio of at least 10:1.

35.        The sensor of claim 29,  
10           wherein at least one of said plurality of beams includes a plurality of  
vertical plates formed therein;  
             wherein said first wafer layer is formed of <100 oriented silicon crystal;  
and  
             wherein said vertical plates have an aspect ratio of at least 10:1.

15           36.        The sensor of claim 29,  
             wherein at least one of said plurality of beams includes an electronic  
circuit formed therein.

20           37.        The sensor of claim 29,  
             wherein at least one of said plurality of beams includes an electronic  
circuit formed therein; and  
             wherein said first wafer layer is formed of <100> oriented silicon  
crystal.

25           38.        The sensor of claim 29,  
             wherein at least one of said plurality of beams includes an electronic  
circuit formed therein and further includes a plurality of vertical plates formed  
therein.

30           39.        The sensor of claim 29,

TOP SECRET 46T82660

5            wherein at least one of said plurality of beams includes an electronic circuit formed therein and further includes a plurality of vertical plates formed therein; and

             wherein said first wafer layer is formed of <100> oriented silicon crystal.

10

40.        The sensor of claim 29,

             wherein at least one of said plurality of beams includes an electronic circuit formed therein and further includes a plurality of vertical plates formed therein; and

15

             wherein said vertical plates have an aspect ratio of at least 10:1.

41.        The sensor of claim 29,

             wherein at least one of said plurality of beams includes an electronic circuit formed therein and further includes a plurality of vertical plates formed therein;

20

             wherein said first wafer layer is formed of <100> oriented silicon crystal; and

             wherein said vertical plates have an aspect ratio of at least 10:1.

25

42.        The sensor of claim 29, wherein each beam has a height of at least 10 microns.

43.        A semiconductor sensor produced by the steps of:

             providing a first single crystal silicon wafer layer;

30

             providing a carrier;

099294-03101  
TOP SECRET

5 including a recessed region bonding the first wafer layer to the carrier  
with the recessed region facing the first wafer layer; and

etching substantially vertically through the first wafer layer opposite the  
recessed region in a curvilinear pattern so as to form a curvilinear structure  
integral with the first wafer layer and suspended over the recessed region.

10

44. The product of claim 43 wherein the step of etching includes  
reactive ion etching.

15

45. The product of claim 43 wherein the step of providing the first  
wafer layer includes providing a single crystal <100> oriented silicon wafer  
layer.

20

46. The product of claim 43 wherein said process includes the  
further step of thinning the first wafer layer to not less than ten microns.

25

47. A semiconductor sensor produced by the steps of:  
providing a first single crystal silicon wafer layer;  
providing a carrier including a recessed region bonding the first wafer  
layer to the carrier with the recessed region facing the first wafer layer; and  
etching substantially vertically through the first wafer layer opposite the  
recessed region so as to form a beam integral with the first wafer layer and  
suspended over the recessed region wherein the beam has an aspect ratio of  
height to width of at least 5:1.

30

48. The product of claim 47 wherein the step of etching includes  
reactive ion etching.

0993194-1343

5           49.     The product of claim 47 wherein the step of providing the first  
wafer layer includes providing a single crystal <100> oriented silicon wafer  
layer.

10           50.     The product of claim 47 wherein the step of etching includes  
etching substantially vertically through the first wafer layer opposite the  
recessed region so as to form multiple beams integral with the first wafer layer  
and suspended over the recessed region wherein each beam has an aspect ratio  
of height to width of at least 10:1.

15           51.     A semiconductor sensor produced by the steps of:  
providing a first single crystal silicon wafer layer  
providing a carrier including a recessed region fusion bonding the first  
wafer layer to the carrier with the recessed region facing the first wafer layer;  
and  
20           etching substantially vertically through the first wafer layer opposite the  
recessed region so as to form a plate integral with the first wafer layer and  
suspended over the recessed region wherein the plate has an aspect ratio of  
height to width of at least 5:1.

25           52.     The product of claim 51 wherein the step of etching includes  
reactive ion etching.

30           53.     The product of claim 51 wherein the step of providing the first  
wafer layer includes providing a single crystal <100> oriented silicon wafer  
layer.

46T.32660

- 5            54.     The product of claim 51 wherein the step of etching includes etching substantially vertically through the first wafer layer opposite the recessed region so as to form multiple plates integrated with the first wafer layer and suspended over the recessed region wherein each plate has an aspect ratio of height to width of at least 10:1.

10

FOI# 4672263